

# MEMORY

## Unbuffered

# 1 M × 64 BIT

# HYPER PAGE MODE DRAM SO-DIMM

## MB8501E064AB-60/-70/-60L/-70L

144-pin, 1 M × 64 Bit Hyper Page Mode SO-DIMM, 3.3 V, 1-bank, 4 KR

### ■ DESCRIPTION

The Fujitsu MB8501E064AB is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of four MB81V16165A devices. The MB8501E064AB is optimized for those applications requiring small size package, low power consumption, enhanced performance. The operation and electrical characteristics of the MB8501E064AB are the same as the MB81V16165A which features hyper page mode (EDO) operation. For ease of memory expansion, the MB8501E064AB is offered in an 144-pin Small Outline Dual In-line Memory Module package (SO-DIMM).

### ■ PRODUCT LINE & FEATURES

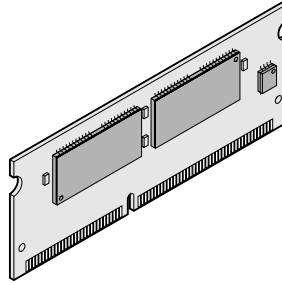
Parameter	MB8501E064AB			
	-60	-60L	-70	-70L
RAS Access Time	60 ns max.		70 ns max.	
Random Cycle Time	104 ns min.		124 ns min.	
Address Access Time	30 ns max.		35 ns max.	
CAS Access Time	15 ns max.		17 ns max.	
Hyper Page Mode Cycle Time	25 ns min.		30 ns min.	
Power Dissipation (max.)	Operating Mode		1152 mW	
	Standby Mode	28.8 mW	14.4 mW	28.8 mW

- Conformed to 144-pin SO-DIMM JEDEC standard
- Organization: 1,048,576 words × 64 bits
- Module Size: 1.00" (height) × 2.66" (length) × 0.15" (thickness)
- Memory: MB81V16165A (1 M × 16, 4 K ref., 3.3 V), 4 pcs
- 3.3 V ± 0.3 V Supply Voltage
- 4,096 Refresh Cycles/65.6 ms
- Hyper Page Operation (EDO)
- Serial Presence Detect (Serial EEPROM)
- RAS Only Refresh/CAS-before-RAS Refresh

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## ■ PACKAGE

144-pin plastic SO DIMM (socket type)



(MDS-144P-P01)

### Package and Ordering Information

– 144-pin SO DIMM, order as MB8501E064AB-xxDG (DG = Gold Pad)

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## ■ PIN ASSIGNMENTS

Pin No.	MB8501E064AB	Pin No.	MB8501E064AB	Pin No.	MB8501E064AB	Pin No.	MB8501E064AB
1	V <sub>SS</sub>	37	DQ <sub>8</sub>	73	$\overline{\text{OE}}$	109	A <sub>9</sub>
2	V <sub>SS</sub>	38	DQ <sub>40</sub>	74	N.C.	110	N.C.
3	DQ <sub>0</sub>	39	DQ <sub>9</sub>	75	V <sub>SS</sub>	111	A <sub>10</sub>
4	DQ <sub>32</sub>	40	DQ <sub>41</sub>	76	V <sub>SS</sub>	112	N.C.
5	DQ <sub>1</sub>	41	DQ <sub>10</sub>	77	N.C.	113	V <sub>CC</sub>
6	DQ <sub>33</sub>	42	DQ <sub>42</sub>	78	N.C.	114	V <sub>CC</sub>
7	DQ <sub>2</sub>	43	DQ <sub>11</sub>	79	N.C.	115	$\overline{\text{CAS}}_2$
8	DQ <sub>34</sub>	44	DQ <sub>43</sub>	80	N.C.	116	$\overline{\text{CAS}}_6$
9	DQ <sub>3</sub>	45	V <sub>CC</sub>	81	V <sub>CC</sub>	117	$\overline{\text{CAS}}_3$
10	DQ <sub>35</sub>	46	V <sub>CC</sub>	82	V <sub>CC</sub>	118	$\overline{\text{CAS}}_7$
11	V <sub>CC</sub>	47	DQ <sub>12</sub>	83	DQ <sub>16</sub>	119	V <sub>SS</sub>
12	V <sub>CC</sub>	48	DQ <sub>44</sub>	84	DQ <sub>48</sub>	120	V <sub>SS</sub>
13	DQ <sub>4</sub>	49	DQ <sub>13</sub>	85	DQ <sub>17</sub>	121	DQ <sub>24</sub>
14	DQ <sub>36</sub>	50	DQ <sub>45</sub>	86	DQ <sub>49</sub>	122	DQ <sub>56</sub>
15	DQ <sub>5</sub>	51	DQ <sub>14</sub>	87	DQ <sub>18</sub>	123	DQ <sub>25</sub>
16	DQ <sub>37</sub>	52	DQ <sub>46</sub>	88	DQ <sub>50</sub>	124	DQ <sub>57</sub>
17	DQ <sub>6</sub>	53	DQ <sub>15</sub>	89	DQ <sub>19</sub>	125	DQ <sub>26</sub>
18	DQ <sub>38</sub>	54	DQ <sub>47</sub>	90	DQ <sub>51</sub>	126	DQ <sub>58</sub>
19	DQ <sub>7</sub>	55	V <sub>SS</sub>	91	V <sub>SS</sub>	127	DQ <sub>27</sub>
20	DQ <sub>39</sub>	56	V <sub>SS</sub>	92	V <sub>SS</sub>	128	DQ <sub>59</sub>
21	V <sub>SS</sub>	57	N.C.	93	DQ <sub>20</sub>	129	V <sub>CC</sub>
22	V <sub>SS</sub>	58	N.C.	94	DQ <sub>52</sub>	130	V <sub>CC</sub>
23	$\overline{\text{CAS}}_0$	59	N.C.	95	DQ <sub>21</sub>	131	DQ <sub>28</sub>
24	$\overline{\text{CAS}}_4$	60	N.C.	96	DQ <sub>53</sub>	132	DQ <sub>60</sub>
25	$\overline{\text{CAS}}_1$	61	N.C.	97	DQ <sub>22</sub>	133	DQ <sub>29</sub>
26	$\overline{\text{CAS}}_5$	62	N.C.	98	DQ <sub>54</sub>	134	DQ <sub>61</sub>
27	V <sub>CC</sub>	63	V <sub>CC</sub>	99	DQ <sub>23</sub>	135	DQ <sub>30</sub>
28	V <sub>CC</sub>	64	V <sub>CC</sub>	100	DQ <sub>55</sub>	136	DQ <sub>62</sub>
29	A <sub>0</sub>	65	N.C.	101	V <sub>CC</sub>	137	DQ <sub>31</sub>
30	A <sub>3</sub>	66	N.C.	102	V <sub>CC</sub>	138	DQ <sub>63</sub>
31	A <sub>1</sub>	67	$\overline{\text{WE}}$	103	A <sub>6</sub>	139	V <sub>SS</sub>
32	A <sub>4</sub>	68	N.C.	104	A <sub>7</sub>	140	V <sub>SS</sub>
33	A <sub>2</sub>	69	$\overline{\text{RAS}}_0$	105	A <sub>8</sub>	141	SDA
34	A <sub>5</sub>	70	N.C.	106	A <sub>11</sub>	142	SCL
35	V <sub>SS</sub>	71	N.C.	107	V <sub>SS</sub>	143	V <sub>CC</sub>
36	V <sub>SS</sub>	72	N.C.	108	V <sub>SS</sub>	144	V <sub>CC</sub>

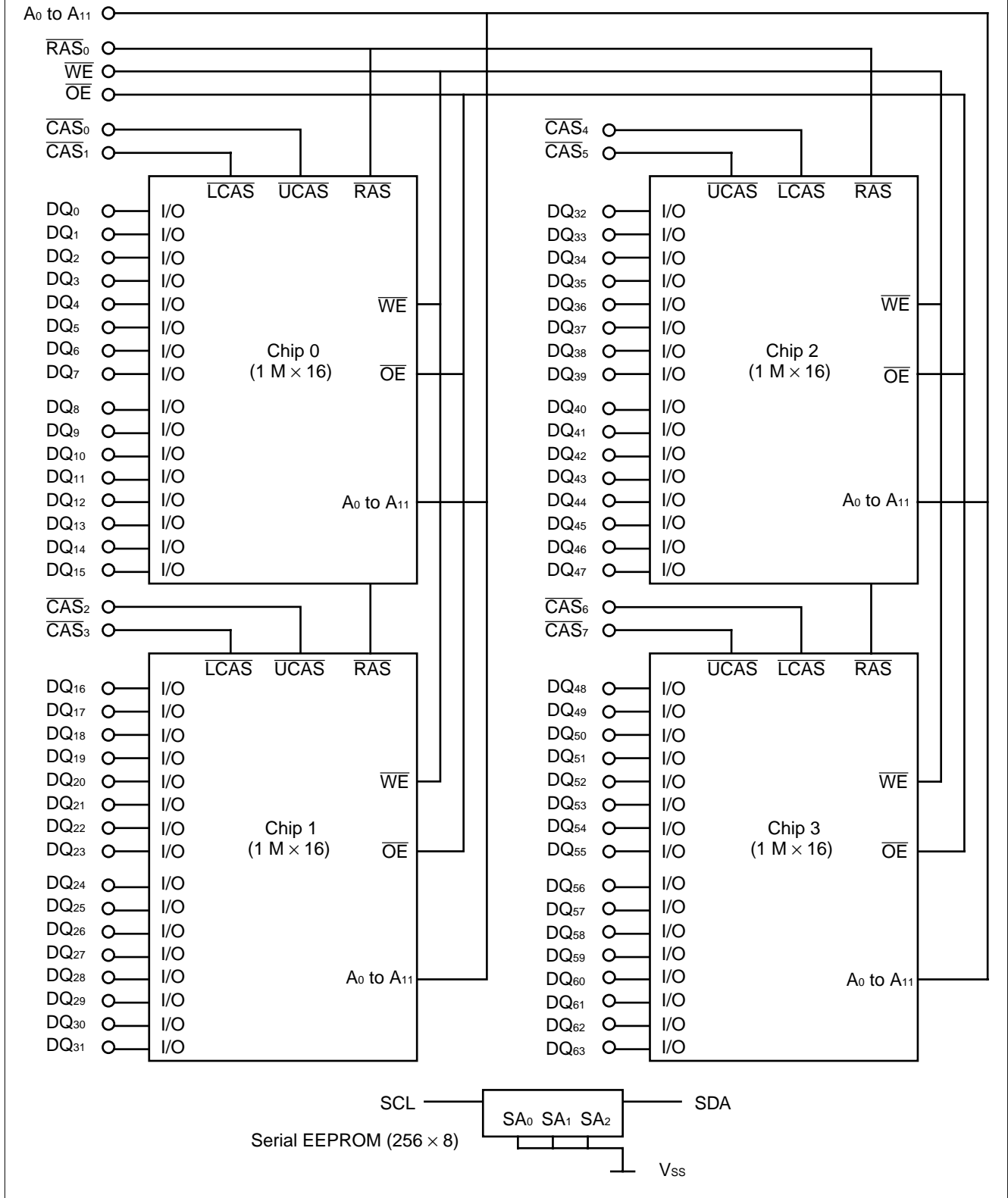
# MB8501E064AB-60/-70/-60L/-70L

## ■ PIN DESCRIPTIONS

Symbol	Function	Input/Output	Pin Count
A <sub>0</sub> to A <sub>11</sub>	Address Input	Input	12
$\overline{\text{RAS}}_0$	Row Address Strobe	Input	1
$\overline{\text{CAS}}_0$ to $\overline{\text{CAS}}_7$	Column Address Strobe	Input	8
$\overline{\text{WE}}$	Write Enable	Input	1
$\overline{\text{OE}}$	Output Enable	Input	1
DQ <sub>0</sub> to DQ <sub>63</sub>	Data-input/Data-output	Input/Output	64
SCL	Serial PD Clock	Input	1
SDA	Serial PD I/O	Input/Output	1
V <sub>CC</sub>	Power Supply	—	18
V <sub>SS</sub>	Ground	—	18
N.C.	No Connection	—	19

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Fig.1 - BLOCK DIAGRAM



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## ■ SERIAL PRESENCE DETECT (SPD) TABLE

Byte	Function Described		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Number of Bytes Used by Module Manufacturer	14 Bytes	0	0	0	0	1	1	1	0
1	Total SPD Memory Size	256 Bytes	0	0	0	0	1	0	0	0
2	Memory Type	EDO	0	0	0	0	0	0	1	0
3	Number of Row Addresses	12 Addresses	0	0	0	0	1	0	0	0
4	Number of Column Addresses	8 Addresses	0	0	0	0	1	0	0	0
5	Number of Banks	1 Bank	0	0	0	0	0	0	0	1
6	Module Data Width (1)	64 Bits	0	1	0	0	0	0	0	0
7	Module Data Width (2)	+0 Bits	0	0	0	0	0	0	0	0
8	Module Interface Levels	LVTTTL	0	0	0	0	0	0	0	1
9	$\overline{\text{RAS}}$ Access Time ( $t_{\text{RAC}}$ )	60 ns	0	0	1	1	1	1	0	0
		70 ns	0	1	0	0	0	1	1	0
10	$\overline{\text{CAS}}$ Access Time ( $t_{\text{CAC}}$ )	15 ns	0	0	0	0	1	1	1	1
		17 ns	0	0	0	1	0	0	0	1
11	Module Configuration Type (Parity or ECC or None)	None	0	0	0	0	0	0	0	0
12	Refresh Rate/ Type	Normal, Self Refresh	1	0	0	0	0	0	0	0
		Low Power, Self Refresh	1	0	0	0	0	0	1	1
13	DRAM Width	×16	0	0	0	1	0	0	0	0
14	Error Checking DRAM Data Width	None	0	0	0	0	0	0	0	0
15 to 31	Reserved for Future Offerings	—	—	—	—	—	—	—	—	—
32 to 63	Superset Information	—	—	—	—	—	—	—	—	—
64 to 127	Manufacturer's Information	—	—	—	—	—	—	—	—	—
128 to 255	Unused Storage Locations	—	—	—	—	—	—	—	—	—

**Note:** Any write operation must NOT be executed into the addresses of Byte 0 to Byte 127. Some or all data stored into Byte 0 to Byte 127 may be broken.

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## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.5 to +4.6	V
Input Voltage	$V_{IN}$	-0.5 to +4.6	V
Output Voltage	$V_{OUT}$	-0.5 to +4.6	V
Short Circuit Output Current	$I_{OUT}$	-50 to +50	mA
Power Dissipation	$P_D$	4	W
Storage Temperature	$T_{STG}$	-55 to +125	°C

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

(Referenced to  $V_{SS}$ )

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
Ground	$V_{SS}$	—	0	0	V
Input High Voltage, All Inputs	$V_{IH}$	2.0	—	$V_{CC} + 0.3 V$	V
Input Low Voltage, All Inputs*	$V_{IL}$	-0.3	—	0.8	V
Ambient Temperature	$T_A$	0	—	+70	°C

**Note:** \* Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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## ■ CAPACITANCE

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{CC} = +3.3\text{ V}$ )

Parameter		Symbol	Value		Unit
			Min.	Max.	
Input Capacitance	$A_0$ to $A_{11}$	$C_{IN1}$	—	28	pF
	$\overline{RAS}_0$	$C_{IN2}$	—	23	pF
	$\overline{CAS}_0$ to $\overline{CAS}_7$	$C_{IN3}$	—	12	pF
	$\overline{WE}$	$C_{IN4}$	—	24	pF
	$\overline{OE}$	$C_{IN5}$	—	24	pF
	SCL	$C_{IN6}$	—	8	pF
I/O Capacitance	$DQ_0$ to $DQ_{63}$	$C_{DQ}$	—	13	pF
	SDA	$C_{SDA}$	—	8	pF



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## ■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes	Test Condition	Symbol	Min.	Max.		Unit
					-60/-70	-60L/-70L	
Output High Voltage	*1	$I_{OH} = -2.0 \text{ mA}$	$V_{OH}$	2.4	—		V
Output Low Voltage	*1	$I_{OL} = +2.0 \text{ mA}$	$V_{OL}$	—	0.4		V
Input Leakage Current	CAS	$0 \text{ V} \leq V_{IN} \leq V_{CC}$ , $3.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ , $V_{SS} = 0 \text{ V}$ , all other pins not under test = $0 \text{ V}$	$I_{I(L)}$	-10	10		$\mu\text{A}$
	Others			-30	30		
Output Leakage Current		$0 \text{ V} \leq V_{OUT} \leq V_{CC}$ , $3.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ , Data out disabled	$I_{O(L)}$	-10	10		$\mu\text{A}$
Operating Current (Average power supply current)	MB8501E064AB -60/-60L	RAS & CAS cycling, $t_{RC} = \text{min.}$	$I_{CC1}$	—	360		mA
	MB8501E064AB -70/-70L			—	320		
Standby Current (Power supply current)	TTL Level	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$	$I_{CC2}$	—	8	4	mA
	CMOS Level	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$		—	4	0.6	
Refresh Current #1 (Average power supply current)	MB8501E064AB -60/-60L	$\overline{\text{CAS}} = V_{IH}$ , RAS = cycling, $t_{RC} = \text{min.}$	$I_{CC3}$	—	360		mA
	MB8501E064AB -70/-70L			—	320		
Hyper Page Mode Current	MB8501E064AB -60/-60L	RAS = $V_{IL}$ , CAS = cycling, $t_{HPC} = \text{min.}$	$I_{CC4}$	—	360		mA
	MB8501E064AB -70/-70L			—	320		
Refresh Current #2 (Average power supply current)	MB8501E064AB -60/-60L	RAS = cycling, CAS-before-RAS, $t_{RC} = \text{min.}$	$I_{CC5}$	—	360		mA
	MB8501E064AB -70/-70L			—	320		
Battery Backup Current (Average power supply current)	MB8501E064AB -60/-70	RAS = cycling, CAS-before-RAS, $t_{RAS} = \text{min. to } 300 \text{ ns}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$ , $t_{RC} = 16 \mu\text{s}$	$I_{CC6}$	—	4	—	mA
	MB8501E064AB -60L/-70L			—	—	1.2	
Refresh Current #3 (Average power supply current)		Self Refresh;	$I_{CC9}$	—	4	1	mA

**Notes:** \*1. Referenced to  $V_{SS}$ .

\*2.  $I_{CC}$  depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

$I_{CC}$  depends on the number of address change as  $\overline{\text{RAS}} = V_{IL}$  and  $\overline{\text{CAS}} = V_{IH}$  and  $V_{IL} > -0.3 \text{ V}$ .

$I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{\text{RAS}} = V_{IL}$  and  $\overline{\text{CAS}} = V_{IH}$ .

$I_{CC2}$  is specified during  $\overline{\text{RAS}} = V_{IH}$  and  $V_{IL} > -0.3 \text{ V}$ .  $I_{CC6}$  is measured on condition that all address signals are fixed steady state.

# MB8501E064AB-60/-70/-60L/-70L

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8501E064AB-60/-60L		MB8501E064AB-70/-70L		Unit
				Min.	Max.	Min.	Max.	
1	Time between Refresh	-60/-70	$t_{REF}$	—	65.6	—	65.6	ms
		-60L/-70L		—	128	—	128	ms
2	Random Read/Write Cycle Time		$t_{RC}$	104	—	124	—	ns
3	Read-Modify-Write Cycle Time		$t_{RWC}$	138	—	162	—	ns
4	Access Time from $\overline{RAS}$	*4, 7	$t_{RAC}$	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	*5, 7	$t_{CAC}$	—	15	—	17	ns
6	Column Address Access Time	*6, 7	$t_{AA}$	—	30	—	35	ns
7	Output Hold Time		$t_{OH}$	3	—	3	—	ns
8	Output Hold Time from $\overline{CAS}$		$t_{OHC}$	5	—	5	—	ns
9	Output Buffer Turn On Delay Time		$t_{ON}$	0	—	0	—	ns
10	Output Buffer Turn Off Delay Time	*8	$t_{OFF}$	—	15	—	17	ns
11	Output Buffer Turn Off Delay Time from $\overline{RAS}$	*8	$t_{OFR}$	—	15	—	17	ns
12	Output Buffer Turn Off Delay Time from $\overline{WE}$	*8	$t_{WEZ}$	—	15	—	17	ns
13	Transition Time		$t_T$	1	50	1	50	ns
14	$\overline{RAS}$ Precharge Time		$t_{RP}$	40	—	50	—	ns
15	$\overline{RAS}$ Pulse Width		$t_{RAS}$	60	100000	70	100000	ns
16	$\overline{RAS}$ Hold Time		$t_{RSH}$	15	—	17	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		$t_{CRP}$	5	—	5	—	ns
18	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*9, 10	$t_{RCD}$	14	45	14	53	ns
19	$\overline{CAS}$ Pulse Width		$t_{CAS}$	10	—	13	—	ns
20	$\overline{CAS}$ Hold Time		$t_{CSH}$	40	—	50	—	ns
21	$\overline{CAS}$ Precharge Time (Normal)	*17	$t_{CPN}$	10	—	10	—	ns
22	Row Address Setup Time		$t_{ASR}$	0	—	0	—	ns
23	Row Address Hold Time		$t_{RAH}$	10	—	10	—	ns
24	Column Address Setup Time		$t_{ASC}$	0	—	0	—	ns
25	Column Address Hold Time		$t_{CAH}$	10	—	10	—	ns
26	Column Address Hold Time from $\overline{RAS}$		$t_{AR}$	24	—	24	—	ns
27	$\overline{RAS}$ to Column Address Delay Time	*11	$t_{RAD}$	12	30	12	35	ns
28	Column Address to $\overline{RAS}$ Lead Time		$t_{RAL}$	30	—	35	—	ns

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No.	Parameter	Notes	Symbol	MB8501E064AB-60/-60L		MB8501E064AB-70/-70L		Unit
				Min.	Max.	Min.	Max.	
29	Column Address to $\overline{\text{CAS}}$ Lead Time		$t_{\text{CAL}}$	23	—	28	—	ns
30	Read Command Setup Time		$t_{\text{RCS}}$	0	—	0	—	ns
31	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	*12	$t_{\text{RRH}}$	0	—	0	—	ns
32	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	*12	$t_{\text{RCH}}$	0	—	0	—	ns
33	Write Command Setup Time	*13, 18	$t_{\text{WCS}}$	0	—	0	—	ns
34	Write Command Hold Time		$t_{\text{WCH}}$	10	—	10	—	ns
35	Write Command Hold Time from $\overline{\text{RAS}}$		$t_{\text{WCR}}$	24	—	24	—	ns
36	$\overline{\text{WE}}$ Pulse Width		$t_{\text{WP}}$	10	—	10	—	ns
37	Write Command to $\overline{\text{RAS}}$ Lead Time		$t_{\text{RWL}}$	15	—	17	—	ns
38	Write Command to $\overline{\text{CAS}}$ Lead Time		$t_{\text{CWL}}$	10	—	13	—	ns
39	DIN Setup Time		$t_{\text{DS}}$	0	—	0	—	ns
40	DIN Hold Time		$t_{\text{DH}}$	10	—	10	—	ns
41	Data Hold Time from $\overline{\text{RAS}}$		$t_{\text{DHR}}$	24	—	24	—	ns
42	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	*18	$t_{\text{RWD}}$	77	—	89	—	ns
43	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	*18	$t_{\text{CWD}}$	32	—	36	—	ns
44	Column Address to $\overline{\text{WE}}$ Delay Time	*18	$t_{\text{AWD}}$	47	—	54	—	ns
45	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles)		$t_{\text{RPC}}$	5	—	5	—	ns
46	$\overline{\text{CAS}}$ Setup Time (C-B-R Refresh)		$t_{\text{CSR}}$	0	—	0	—	ns
47	$\overline{\text{CAS}}$ Hold Time (C-B-R Refresh)		$t_{\text{CHR}}$	10	—	12	—	ns
48	Access Time from $\overline{\text{OE}}$	*7	$t_{\text{OEA}}$	—	15	—	17	ns
49	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	*8	$t_{\text{OEZ}}$	—	15	—	17	ns
50	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data		$t_{\text{OEL}}$	10	—	10	—	ns
51	$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ Lead Time		$t_{\text{COL}}$	5	—	5	—	ns
52	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	*14	$t_{\text{OEH}}$	5	—	5	—	ns
53	$\overline{\text{OE}}$ to Data in Delay Time		$t_{\text{OED}}$	15	—	17	—	ns
54	$\overline{\text{RAS}}$ to Data in Delay Time		$t_{\text{RDD}}$	15	—	17	—	ns
55	$\overline{\text{CAS}}$ to Data in Delay Time		$t_{\text{CDD}}$	15	—	17	—	ns
56	DIN to $\overline{\text{CAS}}$ Delay Time	*15	$t_{\text{DZC}}$	0	—	0	—	ns
57	DIN to $\overline{\text{OE}}$ Delay Time	*15	$t_{\text{DZO}}$	0	—	0	—	ns

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# MB8501E064AB-60/-70/-60L/-70L

(Continued)

No.	Parameter	Notes	Symbol	MB8501E064AB-60/-60L		MB8501E064AB-70/-70L		Unit
				Min.	Max.	Min.	Max.	
58	$\overline{OE}$ Precharge Time		$t_{OEP}$	8	—	8	—	ns
59	$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$		$t_{OECH}$	10	—	10	—	ns
60	$\overline{WE}$ Precharge Time		$t_{WPZ}$	8	—	8	—	ns
61	$\overline{WE}$ to Data in Delay Time		$t_{WED}$	15	—	17	—	ns
62	Hyper Page Mode $\overline{RAS}$ Pulse Width		$t_{RASP}$	—	100000	—	100000	ns
63	Hyper Page Mode Read/Write Cycle Time		$t_{HPC}$	25	—	30	—	ns
64	Hyper Page Mode Read-Modify-Write Cycle Time		$t_{HPRWC}$	69	—	79	—	ns
65	Access Time from $\overline{CAS}$ Precharge	*7, 16	$t_{CPA}$	—	35	—	40	ns
66	Hyper Page Mode $\overline{CAS}$ Precharge Time		$t_{CP}$	10	—	10	—	ns
67	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		$t_{RHCP}$	35	—	40	—	ns
68	Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	*18	$t_{CPWD}$	52	—	59	—	ns
69	$\overline{RAS}$ Pulse Width (Self Refresh)	*19	$t_{RASS}$	100	—	100	—	$\mu s$
70	$\overline{RAS}$ Precharge Time (Self Refresh)	*19	$t_{RPS}$	104	—	124	—	ns
71	$\overline{CAS}$ Hold Time (Self Refresh)	*19	$t_{CHS}$	-50	—	-50	—	ns

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- Notes:**
- \*1. An initial pause ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{IH}}$ ) of 200  $\mu\text{s}$  is required after power-up followed by any eight  $\overline{\text{RAS}}$ -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles are required instead of eight  $\overline{\text{RAS}}$  cycles.
  - \*2. AC characteristics assume  $t_{\text{T}} = 2 \text{ ns}$ .
  - \*3.  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring the timing of input signals. Transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max).
  - \*4. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$ ,  $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$ . If  $t_{\text{RCD}}$  and/or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will be increased by the amount that  $t_{\text{RCD}}$  and/or  $t_{\text{RAD}}$  exceeds the value shown.
  - \*5. If  $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max})$ ,  $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$ , and  $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$ , access time is  $t_{\text{CAC}}$ .
  - \*6. If  $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$  and  $t_{\text{ASC}} \leq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$ , access time is  $t_{\text{AA}}$ .
  - \*7. Measured with a load equivalent to two TTL loads and 100 pF.
  - \*8.  $t_{\text{OFF}}$ ,  $t_{\text{OEZ}}$ ,  $t_{\text{OFR}}$  and  $t_{\text{WEZ}}$  are specified that output buffer change to high-impedance state.
  - \*9. Operation within the  $t_{\text{RCD}} (\text{max})$  limit ensures that  $t_{\text{RAC}} (\text{max})$  can be met.  $t_{\text{RCD}} (\text{max})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}} (\text{max})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$  or  $t_{\text{AA}}$ .
  - \*10.  $t_{\text{RCD}} (\text{min}) = t_{\text{RAH}} (\text{min}) + 2 t_{\text{T}} + t_{\text{ASC}} (\text{min})$ .
  - \*11. Operation within the  $t_{\text{RAD}} (\text{max})$  limit ensures that  $t_{\text{RAC}} (\text{max})$  can be met.  $t_{\text{RAD}} (\text{max})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}} (\text{max})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$  or  $t_{\text{AA}}$ .
  - \*12. Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a read cycle.
  - \*13.  $t_{\text{WCS}}$  is specified as a reference point only. If  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$  the data output pin will remain High-Z state through entire cycle.
  - \*14. Assumes that  $t_{\text{WCS}} < t_{\text{WCS}} (\text{min})$ .
  - \*15. Either  $t_{\text{DZC}}$  or  $t_{\text{DZO}}$  must be satisfied.
  - \*16.  $t_{\text{CPA}}$  is access time from the selection of a new column address (caused by changing  $\overline{\text{CAS}}$  from "L" to "H"). Therefore, if  $t_{\text{CP}}$  becomes long,  $t_{\text{CPA}}$  also becomes longer than  $t_{\text{CPA}} (\text{max})$ .
  - \*17. Assumes that  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh.
  - \*18.  $t_{\text{WCS}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$ , and  $t_{\text{CPWD}}$  are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$ , the cycle is an early write cycle and  $D_{\text{OUT}}$  pin will maintain high-impedance state throughout the entire cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ , and  $t_{\text{CPWD}} \geq t_{\text{CPWD}} (\text{min})$ , the cycle is a read-modify-write cycle and data from the selected cell will appear at the  $D_{\text{OUT}}$  pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the  $D_{\text{OUT}}$  pin, and write operation can be executed by satisfying  $t_{\text{RWL}}$ ,  $t_{\text{CWL}}$ ,  $t_{\text{RAL}}$  and  $t_{\text{CAL}}$  specifications.
  - \*19. Assumes that self refresh.

\*Source: See MB81V16165A Data Sheet for details on the electricals.

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## ■ SERIAL PRESENCE DETECT (SPD) FUNCTION

### 1. PIN DESCRIPTIONS

#### SCL (Serial Clock)

SCL input is used to clock all data input/output of SPD.

#### SDA (Serial Data)

SDA is a common pin used for all data input/output of SPD. The SDA pull-up resistor is required due to the open-drain output.

#### SA<sub>0</sub>, SA<sub>1</sub>, SA<sub>2</sub> (Address)

Address inputs are used to set the least significant three bits of the eight bits slave address. The address inputs must be fixed to select a particular module and the fixed address of each module must be different each other. For this module, any address inputs are not required because all addresses (SA<sub>0</sub>, SA<sub>1</sub>, SA<sub>2</sub>) are driven to V<sub>SS</sub> on the module.

### 2. SPD OPERATIONS

#### CLOCK and DATA CONVENTION

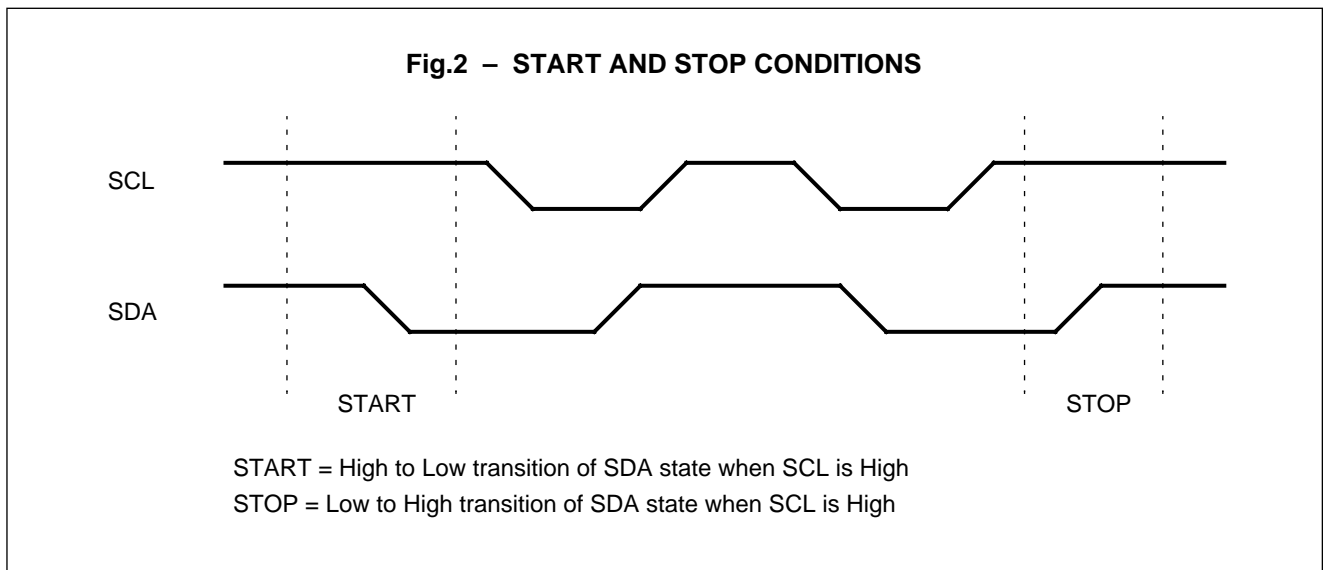
Data states on the SDA can change only during SCL = Low. SDA state changes during SCL = High are indicated start and stop conditions. Refer to Fig.2 below.

#### START CONDITION

All commands are preceded by a start condition, which is a transition of SDA state from High to Low when SCL = High. SPD will not respond to any command until this condition has been met.

#### STOP CONDITION

All read or write operation must be terminated by a stop condition, which is a transition of SDA state from Low to High when SCL = High. The stop condition is also used to make the SPD into the state of standby power mode after a read sequence.



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## ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will put the SDA line to Low in order to acknowledge that it received the eight bits of data.

The SPD will respond with an acknowledge when it received the start condition followed by slave address issued by master.

In the read operation, the SPD will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is issued by master, the SPD will continue to transmit data. If an acknowledge is not detected, the SPD will terminate further data transmissions. The master must then issue a stop condition to return the SPD to the standby power mode.

In the write operation, upon receipt of eight bits of data the SPD will respond with an acknowledge, and await the next eight bits of data, again responding with an acknowledge until the stop condition is issued by master.

## SLAVE ADDRESS ADDRESSING

Following a start condition, the master must output the eight bits slave address. The most significant four bits of the slave address are device type identifier. For the SPD this is fixed as 1010[B]. Refer to the Fig.3 below.

The next three significant bits are used to select a particular device. A system could have up to eight SPD devices—namely up to eight modules—on the bus. The eight addresses for eight SPD devices are defined by the state of the SA0, SA1 and SA2 inputs. For this module, the three bits are fixed as 000[B] because all addresses are driven to V<sub>SS</sub> on the module. Therefore, no address inputs are required.

The last bit of the slave address defines the operation to be performed. When R/ $\bar{W}$  bit is "1", a read operation is selected, when R/ $\bar{W}$  bit is "0", a write operation is selected.

Following the start condition, the SPD monitors the SDA line comparing the slave address being transmitted with its slave address (device type and state of SA<sub>0</sub>, SA<sub>1</sub>, and SA<sub>2</sub> inputs). Upon a correct compare the SPD outputs an acknowledge on the SDA line. Depending on the state of the R/ $\bar{W}$  bit, the SPD will execute a read or write operation.

**Fig.3 – SLAVE ADDRESS**

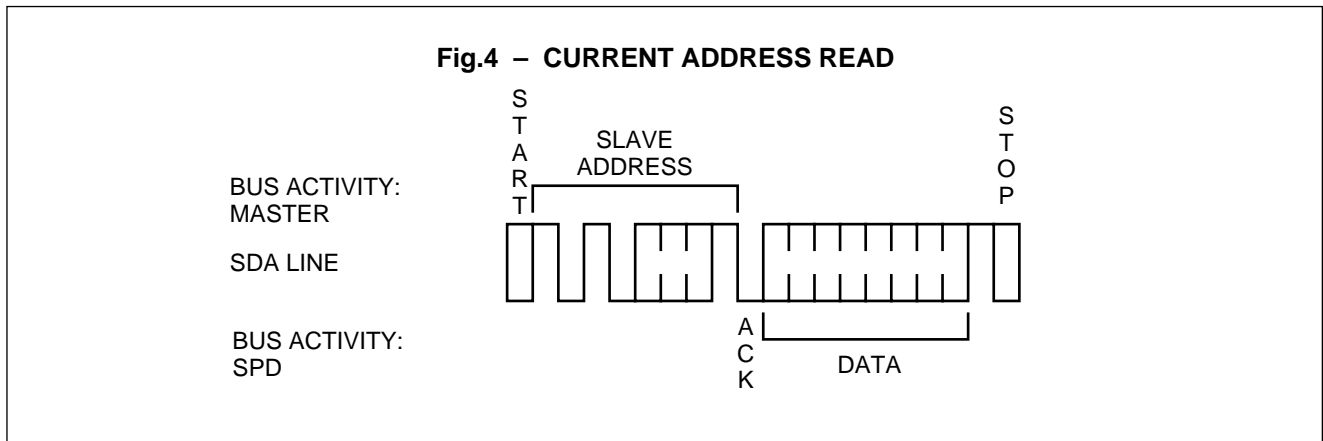
DEVICE TYPE IDENTIFIER				DEVICE ADDRESS			
1	0	1	0	SA <sub>2</sub>	SA <sub>1</sub>	SA <sub>0</sub>	R/ $\bar{W}$

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## 3. READ OPERATIONS

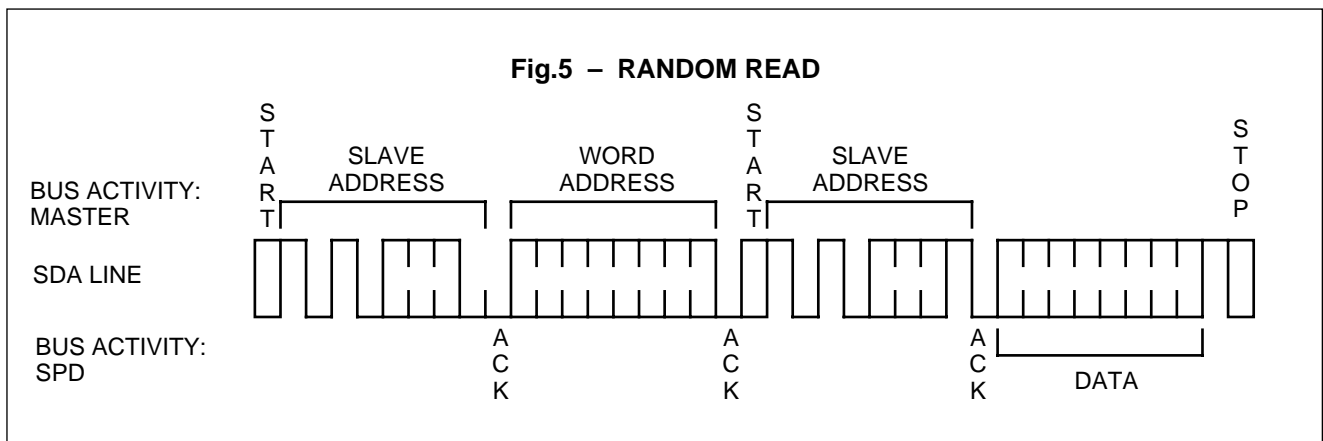
### CURRENT ADDRESS READ

Internally the SPD contains an address counter that maintains the address of the last data accessed, incremented by one. Therefore, if the last access (either a read or write operation) was to address(n), the next read operation would access data from address(n+1). Upon receipt of the slave address with the R/W bit = "1", the SPD issues an acknowledge and transmits the eight bits of data during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig.4 for the sequence of address, acknowledge and data transfer.



### RANDOM READ

Random Read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit = "1", the master must first perform a "dummy" write operation on the SPD. The master issues the start condition, and the slave address followed by the word address. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit = "1". This will be followed by an acknowledge from the SPD and then by the eight bits of data. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig.5 for the sequence of address, acknowledge and data transfer.



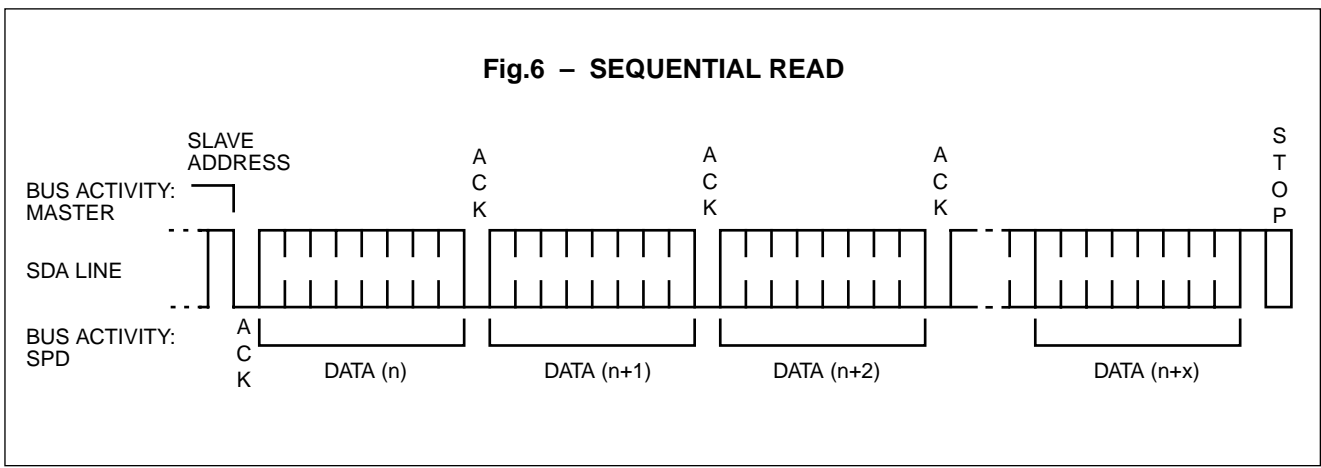


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## SEQUENTIAL READ

Sequential Read can be initiated as either a current address read or random read. The first data are transmitted as with the other read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The SPD continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig.6 for the sequence of address, acknowledge and data transfer.

The data output is sequential, with the data from address (n) followed by the data from address (n+1). The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter "rolls over" to address 0 and the SPD continues to output data for each acknowledge received.



## 4. DC CHARACTERISTICS

Parameter	Note	Test Condition	Symbol	Min.	Max.	Unit
Input Leakage Current		$0\text{ V} \leq V_{IN} \leq V_{CC}$	$S_{ILI}$	-10	10	$\mu\text{A}$
Output Leakage Current		$0\text{ V} \leq V_{OUT} \leq V_{CC}$	$S_{ILO}$	-10	10	$\mu\text{A}$
Output Low Voltage	*1	$I_{OL} = 3.0\text{ mA}$	$S_{VOL}$	—	0.4	V

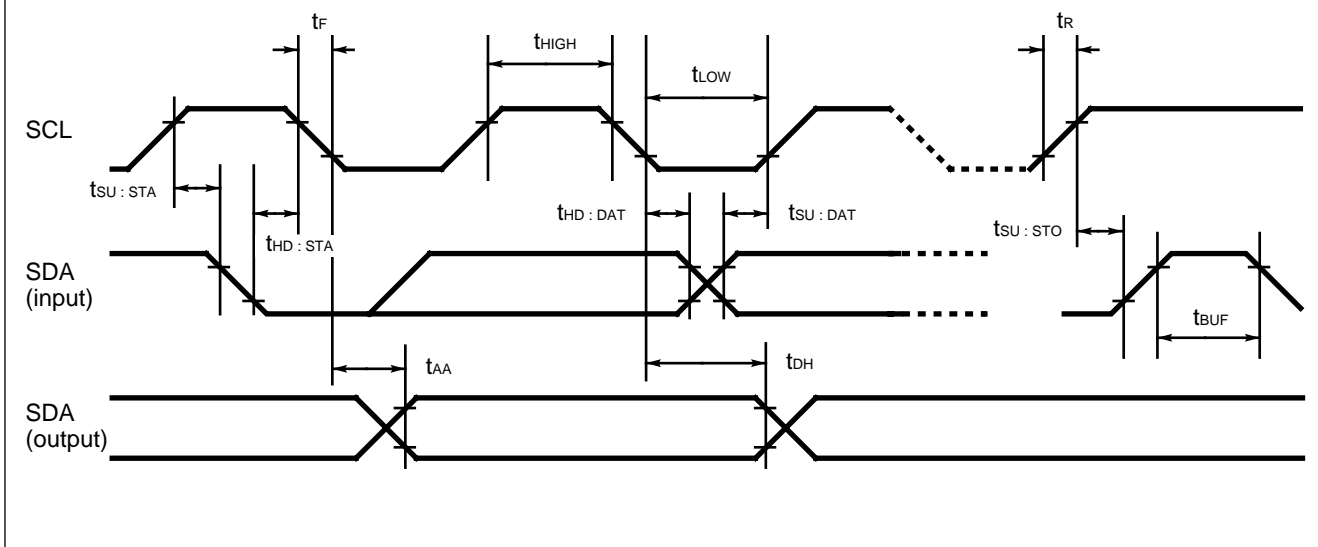
**Note:** \*1.Referenced to  $V_{SS}$ .

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## 5. AC CHARACTERISTICS

No.	Parameter	Symbol	Min.	Max.	Unit
1	SCL Clock Frequency	$f_{SCL}$	0	100	KHz
2	Noise Suppression Time Constant at SCL, SDA Inputs	$T_I$	—	100	ns
3	SCL Low to SDA Data Out Valid	$t_{AA}$	0.3	3.5	$\mu s$
4	Time the Bus must be Free before a New Transmission can Start	$t_{BUF}$	4.7	—	$\mu s$
5	Start Condition Hold Time	$t_{HD:STA}$	4.0	—	$\mu s$
6	Clock Low Period	$t_{LOW}$	4.7	—	$\mu s$
7	Clock High Period	$t_{HIGH}$	4.0	—	$\mu s$
8	Start Condition Setup Time	$t_{SU:STA}$	4.7	—	$\mu s$
9	Data In Hold Time	$t_{HD:DAT}$	0	—	$\mu s$
10	Data In Setup Time	$t_{SU:DAT}$	250	—	ns
11	SDA and SCL Rise Time	$t_R$	—	1	$\mu s$
12	SDA and SCL Fall Time	$t_F$	—	300	ns
13	Stop Condition Setup Time	$t_{SU:STO}$	4.7	—	$\mu s$
14	Data Out Hold Time	$t_{DH}$	100	—	ns
15	Write Cycle Time	$t_{WR}$	—	15	ms

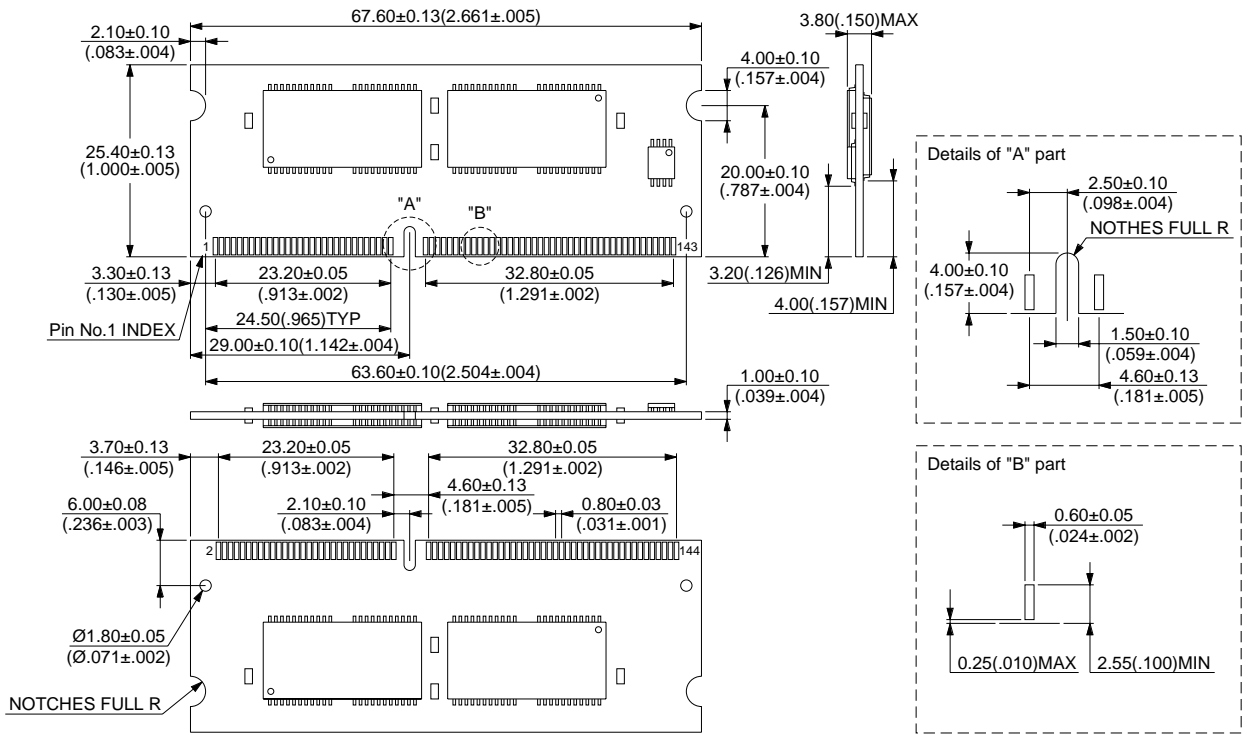
Fig.7 - TIMING WAVEFORM



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## ■ PACKAGE DIMENSIONS

144-pin plastic SO DIMM (socket type)  
(MDS-144P-P01)



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Dimensions in mm (inches)

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